REMARKS

The Final Office Action mailed August 22, 2001, has been received and reviewed. Claims 1 through 4 and 15 through 25 are currently pending in the application. Claims 1 through 4 and 15 through 25 stand rejected. Applicant proposes to amend claim 1 to correct errors in the text. Applicant respectfully requests reconsideration of the application in light of the arguments and remarks set forth below.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,757,078 to Matsuda et al.

Claims 1 through 4, 15 through 17, and 19 through 25 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Matsuda et al. (U.S. Patent No. 5,757,078). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).\

Claims 1 through 4

Independent claim 1 of the presently claimed invention is directed to an apparatus for routing interconnections among bond pads on a semiconductor die. The apparatus includes a sheet like, non-conductive structure having a first surface and a second surface for attachment to a semiconductor die. A plurality of electrically conductive discrete pads are attached to the first surface of the sheet-like, nonconductive structure. The plurality of electrically conductive discrete pads each include an electrical connect portion and a portion facing the first surface with *each discrete pad being electrically isolated about its respective portion facing the first surface of the sheet-like nonconductive structure.*

The Examiner cites Matsuda as teaching all of the limitations of independent claim 1. Particularly, the Examiner points to FIGS. 1 and 2 of Matsuda and states that Matsuda discloses a semiconductor die including a sheet-like nonconductive structure (23) having a first surface, and a second surface for attachment to the semiconductor die (21); and a plurality of electrically conductive discrete pads each having an electrical connection portion and a portion facing the first surface, each being electrically isolated about the portion facing the first surface.

Applicant respectfully submits that Matsuda fails to disclose every element as set forth in independent claim 1. Particularly, Matsuda fails to disclose a plurality of electrically conductive discrete pads having an electrical connection portion and a portion facing the first surface of the sheet-like nonconductive structure, with *each discrete pad being electrically isolated about the portion facing the first surface.*

Matsuda is directed to a semiconductor device package. The package disclosed by Matsuda includes a semiconductor die (21) coupled with a plurality of insulating film layers (25a-25c) through means of an adhesive agent (23). Wiring patterns (29) are formed between each film layer and are electrically interconnected from one layer to another by way of conductive vias. Thus, the semiconductor chip is electrically connected to a plurality of conductive bumps by means of the layered wiring patterns and conductive vias.

The conductive bumps (31) are not electrically isolated about their respective surface facing portions as they are each connected to a wiring pattern (29) by a conductive via. Additionally, the wiring patterns (29) may not be classified as being electrically isolated on their respective surface facing portions. Rather, each wiring pattern (29) is electrically coupled at its surface facing portion to either another wiring pattern (29), a conductive bump (31), or an electrode pad (22) of the semiconductor device (21).

For example:

> The wiring pattern 29 between the second and third insulating films 25b and 25c are connected to the wiring patterns 29 between the first and second insulating film 25a and 25b via the viahole wiring patterns provided in the second insulating

film 25b. Conductive projections, namely, bumps 31 are formed on the third insulating film 25c as an outermost layer of the insulating layer 25 and electrically connected to the wiring pattens 29 between the second and third insulating films 25b and 25c. The bumps 31 are directly bonded onto a printed circuit board (not shown) or the like and a desired semiconductor device can be constructed." (Col. 4, line 63 through col. 5, line 7).

Thus, Matsuda fails to teach that a *plurality of electrically conductive discrete pads have a portion facing a surface of a sheet-like nonconductive structure, the surface facing portion being electrically isolated thereabout.*

As such, Applicant respectfully submits that Matsuda fails to anticipate claim 1 of the presently claimed invention.

Applicant submits that claims 2 through 4 are also allowable over Matsuda as being dependent from an allowable base claim, as well as for the additional patentable subject matter introduced thereby.

Wit respect to claim 2, Matsuda fails to teach the plurality of discrete pads in their recited configuration, as noted above, and further fails to teach at least one conductor extending between at least two of such pads, wherein the at least one conductor includes at least a portion which is external to the sheet-like nonconductive structure.

With respect to claim 3, Matsuda fails to teach a conductor extending from a bond pad of the die to a discrete pad having a surface facing portion isolated thereabout. Rather, Matsuda teaches a bond pad of the die (referred to therein as a conductor 22) which is coupled with a conductive bump by means of multiple wiring patterns and conductive vias. As set forth above, none of the wiring patterns or the conductive bumps are taught to include a surface facing portion which is electrically isolated thereabout as set forth in the presently claimed invention.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 1 through 4.

Claims 15, 16 and 21

Independent claim 15 is directed to a semiconductor device having a die, including a plurality of cond pads disposed on a surface thereof; an adapter having a first plurality of discrete electrical contacts on a first surface thereof with each being electrically connected to one of the plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, each of the second plurality of discrete electrical contacts having and electrical connection portion and *a die facing portion and each being electrically isolated about the die facing portions*, at least some of the second plurality of discrete electrical contacts being in electrical communication with the first plurality of discrete electrical contacts; and a plurality of conductive bumps, each extending from one of the second plurality of discrete electrical contacts.

The Examiner has cited Matsuda, and particularly FIGS. 1 and 2, as teaching all of the limitations of claim 15 of the presently claimed invention, including an adapter having a first plurality of discrete electrical contacts on a first surface thereof. Applicant respectfully disagrees.

As set forth above, Matsuda teaches a semiconductor device package which includes a semiconductor die coupled with multiple layers of an insulating film. Conductive bumps positioned on the outer most layer of insulating film are electrically connected with the semiconductor die through a plurality of wiring patterns and conductive vias. Neither the conductive bumps nor the wiring patterns include a *surface facing portion which is electrically isolated thereabout* as set forth in claim 15. Thus, Applicant submits that claim 15 is not anticipated by Matsuda.

Additionally, Applicant submits that claims 16 and 21 are allowable as being dependent from an allowable base claim. Further, while the Examiner cites col. 4, line 27 through col. 5, line 65 as teaching the subject matter of claim 16, the Examiner does not point to, and Applicant fails to see, any specific passages teaching a protective coating over at least a portion of the die.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 15, 16 and 21.

Claims 17, 19, 20, and 22 through 24

Independent claim 17 is directed to a semiconductor device. The semiconductor device includes a die having a plurality of bond pads disposed on a first surface thereof; and an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each being electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second plurality of discrete electrical contacts being horizontally remote from at least some of the plurality of bond pads disposed on the first surface of the die, the *at least some of said second plurality of discrete electrical contacts being electrically isolated about a die facing portion thereof*, and at least some other of said second plurality of discrete electrical contacts being electrically connected to said first plurality of discrete electrical contacts.

The Examiner relies on Matsuda as teaching all of the limitations of claim 17 referring specifically to FIGS. 1 and 2, and particularly stating that Matsuda discloses an adapter at both ends of the structure in FIG. 1 which includes a first plurality of electrical contacts on a first surface thereof. However, Applicant submits that Matsuda fails to teach all of the limitations of claim 17.

As set forth above with regard to claim 1, Matsuda teaches a semiconductor device package which includes a semiconductor die coupled with multiple layers of an insulating film. Conductive bumps positioned on the outer most layer of insulating film are electrically connected with the semiconductor die through a plurality of wiring patterns and conductive vias. Neither the conductive bumps nor the wiring patterns include a *surface facing portion which is electrically isolated thereabout* as set forth in claim 17. Thus, Applicant submits that claim 17 is not anticipated by Matsuda.

Applicants further submit that claims 19, 20 and 22 through 24 are allowable as being dependent from an allowable base claim, as well as for the additional patentable subject matter introduced thereby.

With respect to claim 20, Matsuda fails to teach a discrete electrical contact on the adapter which is electrically isolated from the plurality of bond pads disposed on the first surface of the die.

With respect to claim 24, Matsuda fails to teach the adapter as set forth above which further comprises a tape-like structure.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 17, 19, 20 and 22 through 24.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,757,078 to Matsuda et al. and Further in View of U.S. Patent No. 4,712,129 to Orcutt

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda et al. (U.S. Patent No. 5,757,078), as applied to claim 15 above, and further in view of Orcutt (U.S. Patent No. 4,712,129). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 18 is improper because the references relied upon fail to teach or suggest all the limitations of the presently claimed invention.

Claim 18 of the presently claimed invention depends from claim 17. Claim 18 recites that the adapter set forth in claim 17 further comprises a material having a coefficient of thermal expansion substantially matching the coefficient of thermal expansion of the die. The Examiner cites Matsuda as teaching all the limitations of claim 17, and then cites Orcutt as teaching "that the texture and the die have similar TCE in order to prevent cracking between the die and the substrate." (Final Office Action, page 3). Further, the Examiner states that "it would have been obvious of one of ordinary skill in the art at the time of the invention was made to use the matching TCE of Orcutt's in Matsuda et al. in order to prevent the cracking between the die and the substrate." (*Id.*).

As addressed above with respect to claim 17, Matsuda fails to teach or suggest all of the limitations of claim 17. Particularly, Matsuda fails to teach or suggest an adapter which includes *at least some of a second plurality of discrete electrical contacts which are electrically isolated about a die facing portion thereof.* Orcutt likewise fails to teach or suggest such subject matter. Thus, the combination of Matsuda and Orcutt fail to teach all of the limitations of the presently claimed invention as set forth in claim 18.

Additionally, Orcutt discloses a semiconductor device which incorporates a rigid planar member (18) which is adhered to a semiconductor device and includes a textured surface. The rigid planar member is stated to be formed of a material having a coefficient of thermal expansion similar to that of the die (bar 12). Orcutt states that the "textured surface 21 of [rigid planar] member 18 provides a means form mechanically locking the upper surface of the bar 12 to the encapsulating medium, for example, plastic, and controlling the shear stresses caused by differential thermal expansion or contraction of the *plastic* and the bar 12." (Col. 2, lines 55-60, emphasis added). Thus, while Orcutt teaches that it is desirable to prevent thermally induced cracking between the bar (die) and the encapsulating plastic, Orcutt approaches this problem by

creating a surface for greater adhesion by the encapsulating plastic rather than matching coefficients of thermal expansion between the encapsulating material and the die. Orcutt, therefore, can not be viewed as teaching or suggesting an adapter having a similar coefficient of thermal expansion as a die to which it is attached.

Thus, Matsuda and Orcutt fail to teach or suggest all of the limitations of the presently claimed invention as set forth in claim 18. As such, Applicant respectfully requests reconsideration and allowance of claim 18.

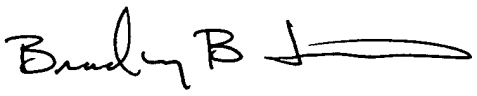
ENTRY OF AMENDMENTS

The proposed amendment to claim 1 above should be entered by the Examiner because the amendment is supported by the as-filed specification and drawings and does not add any new matter to the application. Further, the amendment does not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 4 and 15 through 25 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,



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Date: October 17, 2001
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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Twice Amended) An apparatus for routing interconnections among bond pads on a semiconductor die, comprising:

a sheet-like, nonconductive structure having a first surface, and a second surface for attachment to said semiconductor die; and

a plurality of electrically conductive discrete pads attached to said first surface, the plurality of electrically conductive discrete pads each having an electrical connect portion and a portion facing said first surface, each electrically conductive discrete pad of the plurality being electrically isolated about said portion facing said first surface.